

I CLAIM:

1. An IC fabrication-compatible spiral inductor, comprising
 - a) the inductor having stacked planar coils made from a plurality of spaced conductive layers,
 - b) the stacked planar coils being electrically connected by coil connectors;
 - c) a magnetic core comprising stacked and aligned magnetic elements between the plurality of spaced conductive layers and being located within the stacked planar coils and extending between the spaced metal layers.
2. The inductor of Claim 1 wherein the magnetic element materials are compatible with at least one of CMOS or BiCMOS fabrication technology.
3. The IC fabrication-compatible spiral inductor of Claim 1 wherein the magnetic elements comprise electrically conductive and magnetic material.
4. The IC fabrication-compatible spiral inductor of Claim 1 wherein the coil connectors comprise the same material as the magnetic elements.
5. The IC fabrication-compatible spiral inductor of Claim 4 wherein the magnetic core comprises an array of magnetic element bars within the magnetic core.

6. The inductor according to Claim 5, further comprising a film of magnetic material located at at least one end of the stacked planar coils.

7. The inductor according to Claim 4, further comprising a film of magnetic material located at at least one end of the stacked planar coils.

8. The IC fabrication-compatible spiral inductor of Claim 1 wherein the magnetic core comprises an array of magnetic element bars within the magnetic core.

9. The inductor according to Claim 8, further comprising a film of magnetic material located at at least one end of the stacked planar coils.

10. The inductor according to Claim 1, further comprising a film of magnetic material located at at least one end of the stacked planar coils.

11. The inductor of Claim 1 wherein the inductor has a footprint dimension of about $75\mu\text{m} \times 75\mu\text{m}$ or less.

12. The inductor of Claim 1 wherein the inductor is a 10nH inductor with a footprint dimension of less than $25\mu\text{m} \times 25\mu\text{m}$ in a $0.18\mu\text{m}$ six layer metal interconnect copper CMOS technology.

13. A single chip IC comprising:

- a) a core circuit electrically connected to an inductor;
- b) the inductor having stacked planar coils made from a plurality of spaced layers comprising electrically conductive material,
- c) the stacked planar coils being electrically connected by coil connectors;
- d) the stacked planar coils having a magnetic core comprising stacked and aligned magnetic elements between the plurality of spaced layers and being located within the stacked planar coils.

14. The single chip IC of Claim 13 wherein the magnetic element materials are compatible with at least one of CMOS or BiCMOS fabrication technology.

15. The single chip IC of Claim 13 wherein the magnetic elements comprise electrically conductive and magnetic material.

16. The single chip IC of Claim 15 wherein the coil connectors comprise the same material as the magnetic elements.

17. The single chip IC of Claim 16 wherein the magnetic core comprises an array of magnetic element bars within the magnetic core.

18. The single chip IC according to Claim 17, further comprising a film of magnetic material located at at least one end of the stacked planar coils.

19. The single chip IC according to Claim 16, further comprising a film of magnetic material located at at least one end of the stacked planar coils.

20. The single chip IC of Claim 13 wherein the magnetic core comprises an array of magnetic element bars within the magnetic core.

21. The single chip IC according to Claim 20, further comprising a film of magnetic material located at at least one end of the stacked planar coils.

22. The single chip IC according to Claim 13, further comprising a film of magnetic material located at at least one end of the stacked planar coils.

23. The single chip IC of Claim 13 wherein the inductor has a footprint dimension of about $75\mu\text{m} \times 75\mu\text{m}$ or less.

24. The single chip IC of Claim 13 wherein the inductor is a 10nH inductor with a footprint dimension of $25\mu\text{m} \times 25\mu\text{m}$ in a $0.18\mu\text{m}$ six layer metal interconnect copper CMOS technology.

25. The single chip IC of Claim 15 wherein the electrically conductive and magnetic via material is used for all vias on the IC.

26. The single chip IC of Claim 13 wherein the IC is an RF IC.

27. The single chip IC of Claim 13 wherein the IC is a System on Chip IC.